Stephen F. Roth
Orville R. Cockings
Aaron S. Eckenthal
LERNER, DAVID, LITTENBERG,
KRUMHOLZ & MENTLIK, LLP
600 South Avenue West
Westfield, NJ 07090-1497
Tel: 908.654.5000
Fax: 908.654.7866

Attorneys for Plaintiff Advanced Video Technologies LLC

UNITED STATES DISTRICT COURT
SOUTHERN DISTRICT OF NEW YORK

ADVANCED VIDEO TECHNOLOGIES LLC,	:	**ECF CASE**
	:	
Plaintiff,	:	Civil Action No. 1:11-cv-06604-CM-RLE
v.	:	
	:	District Judge Colleen McMahon
HTC CORPORATION and HTC AMERICA, INC.,	:	Magistrate Judge Ronald L. Ellis
	:	
	:	
Defendants.	:	
	:	
	x	

OPENING CLAIM CONSTRUCTION BRIEF OF
PLAINTIFF ADVANCED VIDEO TECHNOLOGIES LLC

TABLE OF CONTENTS

Page

TABLE OF AUTHORITIES

Page(s)

CASES

I. INTRODUCTION

Pursuant to this Court's Order of January 27, 2012, plaintiff Advanced Video Technologies LLC ("AVT") respectfully submits this opening claim construction brief with regard to those terms of U.S. Patent No. 5,781,788 ("the '788 Patent") that have been identified by the parties as requiring construction by the Court.

II. THE '788 PATENT

The '788 Patent (copy attached to the accompanying Declaration of Orville R. Cockings ("Cockings Decl.") as Exh. A), issued on July 14, 1998, out of an application which was a continuation of an earlier application that was filed on May 8, 1995. The '788 Patent was the subject of a Certificate of Correction (Exh. B), on September 29, 1998, correcting a minor spelling error, and was the subject of reexamination, which resulted in an *ex parte* reexamination certificate (Exh. C), on January 8, 2008.

By way of background, the '788 Patent relates generally to "video compression," which broadly relates to the processing of "video" images. To understand the solution provided by the '788 Patent, it is essential to understand the problem it sought to solve, which is aptly summarized in the "Description Of The Prior Art" in the '788 Patent:

> Television comprises video signals that describe the hue, color saturation and luminance of every picture element (pixel) in a frame at a basic frame rate of thirty frames per second (fps). Each frame can have close to one thousand raster lines each with one thousand individual pixels (720 active pixels per line). Therefore every frame can comprise close to one million pixels. Since thirty fps are typically scanned, close to thirty million pixels per second would ordinarily need to be transmitted from a video camera to a monitor.

(Cockings Decl. Exh. A, 1:22-31.)

Raw video signals contain massive amounts of data. Sending every last bit of this information would take massive computing power and bandwidth, and also require significantly

more storage space. Thus, to allow for efficient transmission and storage of video, it has long been understood that "video compression" is needed.

Broadly speaking, there are at least two established approaches to video compression. One takes advantage of the fact that there is actually a great deal of redundancy between individual video frames. For example, in a video of a sleeping infant, there may be relatively little movement of the infant, and even less movement of the background (*e.g.*, the crib). In this regard, as an object in the video moves, its position within each frame changes. This change in position may be described using a "vector," which is simply a way to describe the direction (*e.g.*, to the left), and magnitude (*e.g.*, how much to the left), of movement using a mathematical pointer. There may be very little difference between one frame and another, and thus a substantial portion of the information in one frame is simply repeated in others. In contrast, if the infant is moving across a floor, video information may change significantly from one frame to the next, greatly reducing the redundancy between frames.

The '788 Patent describes one technique which takes advantage of these principles:

> Motion prediction techniques encode motion vectors and compare the last frame sent, motion-compensated, to the current frame and take the difference. Then only the motion vectors and the difference are transmitted. Obviously for picture subjects that do not move much, such as "talking heads" in video conferencing, the difference information can fall to near zero and an ordinary telephone line could be used to handle the resulting signal bandwidth.

(*Id.* 1:34-40.)

The foregoing approach to video compression can reduce data by representing only the "vectors," reflecting changes from a reference frame to the current frame. The "vector" itself typically requires much less data than the underlying video frames. This is sometimes referred to as reduction of "temporal redundancy." That is, data repeated between frames can be reduced, and under certain conditions eliminated, so long as the "vectors" are retained.

Another approach to video compression takes advantage of "spatial redundancy" within an individual frame. As noted above, "uncompressed" video has, for each frame, thousands of "pixels," each of which may have different coloring and/or brightness. Typically, however, there are redundant areas within a frame, *i.e.*, neighboring areas within a frame that are the same or similar. Reducing spatial redundancy takes advantage of the fact that the human eye is unable to distinguish small differences in color as easily as it can distinguish changes in brightness. Thus, very similar areas of color can be "averaged out." In other words, two adjacent "pixels" having only minor differences in shades of, *e.g.*, the color red, could "split the difference" and be replaced by a single piece of data corresponding to a different "red" that is midway (in terms of frequency or wavelength) between the original two.

While video data can be "compressed" by the foregoing techniques, it also becomes necessary to "decompress" the same data, so that it can be eventually viewed on a monitor or some other video output device, such as a TV. This is analogous to the process of "zipping" and "unzipping" data for review. While these concepts are important to help provide the background to the invention of the '788 Patent, what the invention *does* relate to are improvements which allow us to have affordable devices such as video cameras small enough to fit in our pockets.

Video compression and decompression are typically performed on one or more semiconductor chips. The never-ending goal is to design a chip that can do all the work that is asked of it, while remaining as small as possible. While a chip that can perform processes such as video compression and decompression could also — in theory — be designed to provide the storage space that may be needed in a given device, the desire to include storage on the chip itself would affect product design, *e.g.*, power consumption and size, and cost.

Thus, one important aspect of the invention of the '788 Patent begins with the recognition that a pure storage device, which is not required to perform *other* processes (such as video data compression or decompression) can itself be made relatively cheaply. Existing devices known as "dynamic random access memories" (or "DRAMs") can provide such storage.

Accordingly, a feature of the invention of the '788 Patent is to employ a chip that tackles the compression and decompression tasks, along with a *separate* "off-chip storage" device (*e.g.*, a DRAM) that can receive and store data from the chip, and which can allow the chip to withdraw data from the DRAM as needed for processing.

Thus, as shown in Figure 1 of the '788 Patent, the chip which performs "compression/decompression" (sometimes referred to as "codec") receives data that originates with a video source 14 (*e.g.*, a camera) when the video is shot. (*See*, e.g., Cockings Decl. Exh A, FIG. 1.) The video codec chip 12 has a connection with the DRAM 18 through which the chip stores data at various stages of processing. (*Id.*) The portion of the system of Figure 1 described thus far may be sufficient to envision the use of the system in a handheld video camera or smartphone that includes a video camera. When the video is being shot, signals from the video source 14 go into the video codec chip 12, where the data can be compressed and, as needed, off-loaded to the DRAM 18 during processing. (*Id.*, 3:43-48.)

As a final point, the preferred embodiment of Figure 1 depicted and described above also contemplates the possibility of data being transmitted to a video telephone or remote location, such as through video conferencing. Under this arrangement, the video data (from, *e.g.*, an office in New York) that has been compressed by the video codec 12, is emitted on a "transmit channel" 20 in compressed form. It can be received at another location (*e.g.*, an office in Chicago) having a similar system, on its own similar "receive channel" 22, by which the

compressed data can enter the video codec (in Chicago) for decompression, followed by transmission of the decompressed video signal to a monitor. Other applications contemplated include remote, or off-chip, retrieval of video data from a database or other storage element.

III. THE LEGAL STANDARD

The Federal Circuit has repeatedly held that the "words of a claim 'are generally given their ordinary and customary meaning,'" and "the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005); s*ee also Aventis Pharma v. Hospira*, 2011-1018, 2012 U.S. App. LEXIS 7095 (Fed. Cir. Apr. 9, 2012). It is also well established that the meaning of the claim language must be interpreted in the context of the written description of the invention found in the patent, and the prosecution history. *MySpace, Inc. v. Graphon Corp.*, 672 F.3d 1250 (Fed. Cir. 2012).

The Claim Language. The starting point for any claim construction analysis is the language of the claims themselves, for this language "define[s] the invention to which the patentee is entitled the right to exclude." *Phillip,* 415 F.3d. at 1312.

The Patent Specification. Claims do not stand alone — they are part of "'a fully integrated written instrument,' . . . consisting principally of a specification that concludes with the claims." *Id.* at 1315 (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 978 (Fed. Cir. 1995)). The specification is always highly relevant and usually dispositive; indeed, it "is the single best guide to the meaning of a disputed term." *Marine Polymer Techs. v. HemCon, Inc.* 672 F3d. 1350, 1367 (Fed. Cir. 2012) (quoting *Phillips,* 415 F.3d at 1315).

The Prosecution History. The prosecution history is part of the intrinsic evidence. *Sanofi-Aventis Deutschland GMBH v. Genentech, Inc.*, 2011-1397, 2012 U.S. App. LEXIS 5985, at *13 (Fed. Cir. Mar. 22, 2012). It consists of the complete record of the proceedings before the

PTO and includes the prior art cited during the examination of the patent. *Id*. It also "provides evidence of how the [Patent and Trademark Office] PTO and the inventor understood the patent." *Phillips*, 415 F.3d at 1317. Moreover, it can inform the meaning of the claim language by demonstrating if the inventor limited the invention during the course of prosecution by making the claim scope narrower than it otherwise would be. *Id*. Nevertheless, it should be understood that while the prosecution history can offer insight into the meaning of a particular claim term, the claim language and the specification generally carry greater weight. *HTC Corp. v. IPCom GmbH & Co.*, 667 F.3d 1270, 1276 (Fed. Cir. 2012).

Extrinsic Evidence. The Court may also use extrinsic evidence which is evidence that is external to the patent and prosecution history, to determine the meaning of the claims. *Advanced Fiber Technos. (AFT) Trust v. J&L Fiber Sers., Inc.*, 674 F.3d 1365 (Fed. Cir. 2012). Such evidence may include expert and inventor testimony, dictionaries and learned treatises. *Markman*, 52 F.3d at 980. The Federal Circuit has explained that technical dictionaries may provide the court with a better understanding of the underlying technology and the way in which one of skill in the art might use the claim terms. *Phillips*, 415 F.3d at 1318.

IV. CONSTRUCTION OF IDENTIFIED CLAIM TERMS

There are several asserted claims in the reexamined '788 Patent. (Cockings Decl. Exh. C.) No single claim includes every term that has been identified as requiring construction, although independent claim 13 includes most of the claim terms which the Court will be asked to construe. Thus, we will use that claim as illustrative.

A. "A Single Semiconductor Chip"

The term "a single semiconductor chip" appears early in element [a] of claim 13 in the context of:

13. A video codec, comprising:

[a] **a single semiconductor chip** providing for a video input connection from a camera and a video output connection to a monitor of decompressed data, and a transmit channel and a receive channel of compressed data; [1]

The context of the term itself is highly instructive in informing us that "single" and "semiconductor" are characteristics of the "chip." The surrounding claim language further informs us that the "single semiconductor chip" provides for video input and output connections and transmit and receive channels. The plain language of the term therefore indicates that "single" is meant to specify a structural feature of the "chip" since it's the "single chip" block in the '788 Patent that provides for the connections and channels. Similarly, "semiconductor" refers to the material that the chip is made of.

Figure 1 of the '788 Patent and the first paragraph of the Detailed Description show and describe a single chip video codec 12 that provides the connections recited in the claims. Other portions of the specification consistently refer to the video codec as a "single-chip." (Cockings Decl. Exh. A, Abstract, 1:9-10, 2:5, 2:9, 2:14, 2:21, 2:26, 2:29, 2:40, 3:9-11, 3:16-17.) The specification also discloses that in one embodiment the video codec "comprises video compression and decompression processors, and single-chip architectures." (*Id.* 2:31-35.)

Figure 3 shows a detailed block diagram of the single chip including various processors such as, for example, processors 32, 34, and 38 for performing different functions as part of the compression/decompression process. Each processor is contained within the chip. The processors also use various buses (*e.g.*, delivery subsystem) within the chip to transfer data off chip and communicate with other components within the chip. (*Id.* 7:8-15, 8:21-25, 5:40-45.) Figure 3 also shows the buses, processors, and other circuit components as being interconnected

[1] All boldfacing or italicizing in this brief is added by AVT unless otherwise noted.

within the chip. The various interconnections form an integrated circuit structure within the chip.

Additional insight is provided in connection with the term "single semiconductor chip" by canceled claim 8 of the original '788 Patent. That claim was directed to "**A single-chip** video codec, *comprising*: **a single semiconductor integrated circuit (IC)** with external connections provided for a video source input, a video output, a transmit communications channel, a receive communications channel . . . ." (Cockings Decl. Exh. A, 16:28-35; *see also* Original Prosecution History Exh. D 65-66.) Here, the inventors made it clear that a "single-chip video codec" may be made up of "a single semiconductor integrated circuit." They were careful, however, to distinguish between the term "a single . . . *chip*" and "a single . . . *integrated circuit*." Significantly, while a "single-chip" may comprise "a single . . . integrated circuit," the term "*chip*" is not used synonymously with "*integrated circuit*."

AVT therefore respectfully submits that in view of the intrinsic evidence the proper construction of "a single semiconductor chip" is "**<u>a single chip containing integrated circuitry made of semiconductor material</u>**."

B. <u>"Video Input Data "</u>

The phrase "video input data" appears in element [b] of claim 13:

> **[b]** an interface connected to the chip for external connection to a separate frame memory dynamic random access memory (DRAM) and that provides for interim storage of incoming and outgoing video data, wherein the incoming video data is **video input data** from the video input connection; and

Thus, element [b] addresses the function of the interface in terms of providing for (*inter alia*) "interim storage of incoming . . . video data." The claim language itself expressly tells us that "incoming video data is **video input data**" from the "video input connection." And element [a] tells us that the chip provides for a "video input connection *from a camera*." Thus,

the overall structure of the claim, in and of itself, suggests that "video input data" may be data (having originated with a "camera") that is associated with an image captured by the camera.

The Abstract and other portions of the '788 Patent, provide further helpful guidance in connection with the term "video input data." It reads in pertinent part as follows:

> A single-chip video compression/decompression (video codec) chip is connected to receive a **video input** from a NTSC-compatible or PAL-compatible camera and a transmit channel. **Video information from the camera or other video input source is compressed by the video codec and transmitted out in compressed form on a transmit channel**. . . . Only a separate single module of dynamic random access memory (DRAM) is needed to provide storage for **incoming and outgoing video data**, compressed bit streams and reconstructed pictures for both compression and decompression procedures.

The fact that the data is coming from a camera or another video input source indicates that the data is associated with an image. The Detailed Description of the specification provides still further support. It states as follows:

> FIG. 1 illustrates a video system embodiment of the present invention, referred to by the general reference numeral 10. A single-chip video compression/decompression (video codec) chip 12 is connected to receive a **video input** from a NTSC-compatible or PAL-compatible camera 14 and a monitor 16. ("NTSC" and "PAL" are respective television-broadcast standards used in the United States and Europe.) A separate dynamic random access memory (DRAM) 18 provides storage for **incoming** and outgoing **video data**. **Video information from the camera 14 or other video input source is compressed by the video codec 12 and transmitted out in compressed form on a transmit channel 20**. Conversely, compressed video information is input to the video codec 12 from a receive channel 22, decompressed and output to the monitor 16 or other video output device, e.g., a television set.

(Cockings Decl. Exh. A, 3:36-51.) Here again, as with the Abstract, the specification indicates that the "video input data" is data that is associated with an image.

While image data from a camera is one form of information that may be input to the chip, the specification indicates that "various data rates can be interfaced to the video input/output ports." (*Id.* 6:52-53.) Further, the specification discloses that interactive multimedia and remote

retrieval of data from a database are applications that may utilize the invention. (*Id.*, 1:13-15.) Thus, "video input data" includes various types of video information.

The prosecution history provides further support for AVT's construction. Because the term "video input data" was added during reexamination, AVT does not believe the prosecution of the original '788 Patent is instructive. However, during the reexamination, the importance of "video input data" to the claims was made clear and, indeed, was an important basis upon which the claims were allowed.

During reexamination, the applicants argued that the claims were distinguishable based on what type of information was held in "interim storage." Most significantly, in the amendment that added this language, the patentees argued as follows:

- With respect to Suzuki, they noted, "Even after being updated, the data in coding frame memory 2 is not necessarily the same as image input data 1, because it is reconstructed from compressed data and is therefore prone to including compression artifacts . . . ."

(Cockings Decl. Exh. E, at 263-64, Amendment, Aug. 13, 2007.)

- Indeed, it appears that rather than providing interim storage of uncompressed input/output video data, the frame memory of Suzuki merely provides for storage for reconstructed previous video frame data for use in intermediate stages of processing between being input and output.

(*Id.* at 264.)

- Bose does not specify whether the input video data is buffered in the FIFO and passed directly into the DRAM, or whether the input video data is passed first to the processing components of the chip, such as the motion estimator (which would be in harmony with the operation described in Suzuki).

(*Id.* at 267.)

All in all, these arguments establish that the claims were distinguished on the basis that the "input video data" must be data prior to compression by the video codec. Accordingly, in

light of all of the foregoing, AVT respectfully submits it to be clear that the term "video input data" means "**video data prior to compression by a video codec**."

C. "Video Input Data From The Video Input Connection"/"Video Input Information Received From Said Video Input Connection"

Though the phrases "video input data from the video input connection" and "video input information received from said video input connection" appear to be similar, they appear in different places in the claims and warrant slightly different constructions. Therefore, below AVT addresses each of these terms in separate subparts. In addition, the parties have preliminarily agreed that the term "video input connection" recited within these phrases means "**one or more external connection pins or ports for receiving video data**."

1. "Video Input Data From The Video Input Connection"

In previous subparts, AVT has set forth its views on the proper construction of the separate term "video input data." That meaning (as well as the meaning of "video input connection") must necessarily hold true in the context of the more complete expression "video input data from the video input connection." Accordingly, AVT will in this subpart focus on the meaning of the overall phrase, as well as the word "from."

The first sentence of the Abstract, and the portion of the specification appearing at column 3, lines 36-51, which were quoted above in Part III.B, are also pertinent to the present discussion. By referring to "video information" coming from the camera or other video source, it is clear that what is being "input" through the "connection" is data. Thus, the specification further states, "various data rates can be interfaced to the video input/output ports." (Cockings Decl. Exh. A, 6:53-54.)

That the present limitation involves data entering through one or more "ports" is made clear by this portion of the specification:

> When decoding, the motion predictor 32 reconstructs each video frame by adding a received-frame difference to a frame prediction based on previous reconstructed frames. The motion predictor 32 processes the main bitstreams between the **video input**/output **ports** and the forward/inverse discrete cosine transform transformers. The encoding process is activated by a video input macroblock start signal. The decoding process is activated by a signal from the DCTQ 34.

(*Id.* 6:9-15.) Still further, the notion that the particular type of "ports" may include "pins" is suggested in the specification as follows:

> For a single-chip implementation of the video codec 12, external connection pins should preferably be provided for a clock, a hardware or software reset, an eighteen-bit memory address bus, a thirty-two bit memory data bus, a row select address for DRAM row address strobe that latches the memory address into DRAM's row address registers, a column select address for DRAM column address strobe that latches the memory address into DRAM's column address registers, a memory read enable to activate the memory's output buffer, and a memory write enable to latch memory data into the memory cells selected.

(Cockings Decl. Exh. A, 12:50-60.)

Accordingly, AVT suggests that the proper construction of "video input data from the video input connection" should be "**<u>video data prior to compression by a video codec received at one or more external connection pins or ports</u>**."

2. "Video Information Received <u>From Said Video Input Connection"</u>

The phrase "video input information received from said video input connection" appears later in the claims than the phrase "video input data from the video input connection." In particular, "video input information" appears in element[c] and [e] of claim 13:

> **[c]** a video compressor/decompressor disposed fully within the chip and connected to compress **video information received from said video input connection** for output on said transmit channel, and connected to decompress video information received from said receive channel for output on said video output connection;
>
> . . . .
>
> **[e]** wherein the video compressor/decompressor includes dedicated hardware logic which performs forward discrete cosine transforms on the **video information received from the video input connection** and wherein the same dedicated hardware logic also

performs inverse discrete cosine transforms on the video information received from the receive channel.

The plain language of the claim tells us that the "video input information received from said [or the] video input connection" is to be compressed by the compressor/decompressor within the chip and transformed by the dedicated hardware logic included in the compressor/decompressor. Thus, this video information has moved from the "video input connection" further into the chip, and received by other components within the chip.

The specification discloses that the "discrete cosine transform and quantization (DCTQ) block 34 provides for discrete cosine transform, zigzag conversion and quantization." (Cockings Decl. Exh. A, 5:1-3) The specification also indicates that block 34 receives the video information from input connection after it has gone through some processing by other components within the chip. (*Id.* 6:11-4.)

FIG. 2 shows this operation. In the figure, block 34 receives and transmits information from block 32. The plain meaning of the claim language and the specification therefore indicate that "video input information" may include information at different stages of compression processing — not just prior to compression.

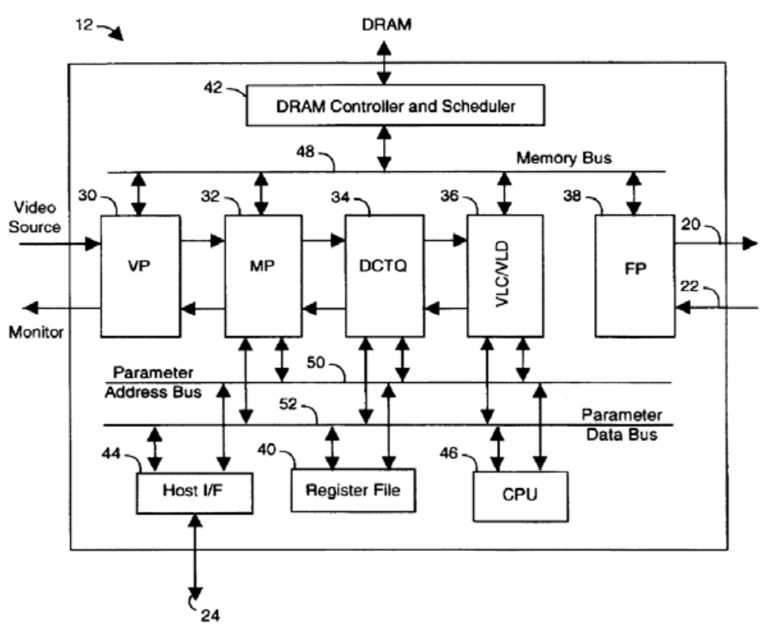

FIG. 2

Accordingly, AVT respectfully submits that properly construed the phrase "video input information received from said [or the] video input connection" means "**<u>video data prior to or</u>**

<u>during compression by a video codec received at one or more external connection pins or parts</u>."

D. <u>"Outgoing Video Data"</u>

The term "outgoing video data" appears in element [b] of claim 13:

> **[b]** an interface connected to the chip for external connection to a separate frame memory dynamic random access memory (DRAM) and that provides for interim storage of incoming and **outgoing video data**, wherein the incoming video data is video input data from the video input connection;

The context of the surrounding claim language and the overall structure of the asserted claims are highly instructive in determining the construction of "outgoing video data." The claim language itself instructs us that the "video data" is "outgoing." This strongly implies that the term refers to video data that is being sent *from* the chip.

Further, element [a] recites that the chip provides for "*a video output connection* to a monitor *of decompressed data*, and a *transmit channel* . . . *of compressed data*." Element [c] also tells us other components within the chip are "connected to *compress video information* received from said video input connection *for output on said transmit channel*, and connected to *decompress video information* received from said receive channel *for output on said video output connection*." The claims therefore contemplate two types of data being "output" from the chip: (1) compressed video information on the transmit channel; (2) decompressed video information on the video output connection. Within the overall structure of the claim "outgoing video data" thus includes both compressed and decompressed data output from the chip.

The specification clarifies that "outgoing video data" necessarily includes these two types of data. For example, Figure 1 shows the same two types of data being output on a transmit channel 20 and an output connection to a monitor 16. In describing Figure 1, the specification explains:

> A separate dynamic random access memory (DRAM) 18 provides storage for incoming and **outgoing video data**. **Video information** from the camera 14 or other video input source **is compressed by the video codec 12 and transmitted out in compressed form on a transmit channel 20**. **Conversely, compressed video information is** input to the video codec 12 from a receive channel 22, **decompressed and output to the monitor 16 or other video output device, e.g., a television set**.

(Cockings Decl. Exh. A, 3:36-51.)

The Abstract includes similar disclosure. In all instances, the specification makes clear that "outgoing video data" is information that is transmitted or output from the chip. Further, this information may be decompressed or compressed.

AVT therefore respectfully submits that the term "outgoing video data" means "**<u>decompressed or compressed video data</u>**."

E. <u>"Interim Storage Of Incoming And Outgoing Video Data"</u>

This phrase appears in element [b] of claim 13. For convenience, we again reproduce that portion of the claim to show the context:

> **[b]** an interface connected to the chip for external connection to a separate frame memory dynamic random access memory (DRAM) and that provides for **[1] interim storage of [2] incoming and outgoing video data**, wherein the incoming video data is video input data from the video input connection;

Within the phrase, the term "outgoing video data" has been construed above. Therefore, in this subsection we construe the other terms that make up the phrase, *i.e.*, "interim storage" and "incoming . . . video data."

1. <u>"Interim Storage Of"</u>

The term "interim storage" is used in the claims in connection with storing incoming and outgoing video data that is processed by the claimed codec and output as either compressed or decompressed data. Such data is thus not permanently stored in the chip or on the DRAM. Moreover, the reference to outgoing video data makes clear that the claim by no means contemplates the storage being anything but temporary.

Other than in the claims themselves, the term "interim storage" does not appear in the specification of the '788 Patent. The specification does, however, describe buffers that are used to store incoming and outgoing video data at various stages of processing. (*See, e.g.*, Cockings Decl. Exh. A, 4:63-65, 5:29-34, 6: 59-65.) As indicated by *The New IEEE Standard Dictionary of Electronics Terms* (5th ed. 1993) (hereinafter "*the IEEE Dictionary"*), to the ordinary artisan a buffer is a device used for temporarily storing data. (*See, e.g., id.* Exh. FG, at 135 ("buffer (1) (buffer storage) . . . (A) A device in which data are stored temporarily, in the course of transmission from one point to another. . . .").)[2] This makes clear that the DRAM and codec chip use buffering so that data can be temporarily stored and "fetched" when needed.

Further, *Webster's* defines "interim" as "belonging to an interim : done, made, of occurring for an interim or meantime : TEMPORARY, PROVISIONAL . . . committee . . . government . . . lease." (Cockings Decl. Exh. G, at 1179.) Likewise, *Webster's* defines "storage" as "**1 a:** space for storing . . . available at low rates . . . cabinet . . . room **b :** a place for storing . . . **4 :** MEMORY." (*Id.* at 2252.) A relevant scientific dictionary defines "storage" as "(A) The act of storing information. (B) Any device in which information can be stored, sometimes called a memory device." (Cockings Decl. Exh. F, at 1294-98.)

Although during the reexamination of the '788 Patent there was considerable discussion of "interim storage," that discussion focused not on the meaning of the term, but rather on the type of data that was subject to such storage. (*See, e.g.,* Cockings Decl. Exh. E, at 177-79, (Amendment, Feb. 22, 2007).) What is instructive, however, is that in considering this term, the

[2] A copy of each of the pages of the *IEEE Dictionary* cited herein by AVT is annexed to the Cockings declaration as Exhibit F. Excerpts from *Webster's Third New International Dictionary (Unabridged)* (1986 ed.) (hereinafter "*Webster's*") are annexed to the Cockings declaration as Exhibit G and the *McGraw-Hill Dictionary of Scientific and Technical Terms* (5th ed. 1994) ("*McGraw Hill*") as Exhibit H. The Federal Circuit has noted that within the class of extrinsic evidence, dictionaries can be useful in claim construction. *See Phillips*, 415 F.3d at 1318.

Examiner asserted that the *Suzuki* prior art reference (U.S. Patent No. 5,491,515) stored data "interim to (e.g., prior to) being read out of frame memory." (Cockings Decl. Exh. E, at 199 (Office Action, May 30, 1997).) Thus, the Examiner understood the word "interim" to be used consistently with its ordinary meaning, *i.e.*, not permanent storage but storage prior to passing on data to other stages of processing.

In all, there is nothing in the '788 Patent to suggest that "interim storage" should be construed to mean anything but storage which is provided for some "interim," *i.e.*, storage which is temporary. Accordingly, the proper definition of "interim storage" is "**temporary storage**."

2. "Incoming . . . Video Data"

The term "incoming . . . video data" is used in two different contexts among the asserted claims. Claims 5, 13, and 26 include as a feature "wherein the **incoming video data** **is** *video input data from the video input connection*." When used in this context, the claims cover a specific form of "incoming video data," as represented by the italicized claim language which has been construed above in other subsections.

In contrast, "incoming . . . video data" is not used in the same way in claim 23. In that claim it appears in the second element without the wherein language:

> an interface connected to the chip for external connection to a separate frame memory dynamic random access memory (DRAM) and that provides for interim storage of **incoming** and outgoing **video data**;

As used in this context, "incoming . . . video data" may include data other than "video input data." Therefore, incoming video data should be construed more broadly.

Other elements in claim 23, as well as the other asserted claims, support this interpretation. For example, the first element in claim 23 (as also reflected in element [a] of claim 13 above) instructs us that "incoming video data" may include data from the video input connection or receive channel. The claims also state that the video compressor/decompressor

element is connected "to compress video information received from said video input connection . . . [and] to decompress video information received from the received channel." Other portions of the claims clarify that the video compressor/decompressor transforms the information received on the input connection and receive channel. The claims therefore strongly imply that incoming video data to the chip includes uncompressed and compressed video information.

The specification reinforces this concept. For example, the specification teaches that uncompressed video information from a video source 14, *e.g.*, a video camera, is received and compressed by the chip. (Cockings Decl. Exh. A, 3:45-48.) Conversely, compressed data is inputted on the receive channel 22 and decompressed by the chip. (*Id*. 3:48-51.) Figure 1 shows this configuration of the chip. (*Id.*, FIG. 1.)

Further, the specification describes other components within the chip as being responsible for transforming the video data received by the chip. Those components include discrete cosine transform and quantization (DCTQ) block 34. Block 34 is located within the chip.

The specification explains that during encoding motion predictor 32 supplies "frame-difference data, instead of the frame itself, to the DCTQ 34." (*Id.* 6:1-4.) Further, during decoding the "motion predictor 32 processes the main bit streams between the video input/output ports and the forward/inverse discrete transformers" in block 34. (*Id*. 6:13-15.) Thus, the data and bit streams exchanged between the components within the chip include data at various stages of processing including prior to compression or decompression, and data being compressed or decompressed.

Accordingly, AVT respectfully submits that the proper construction of "incoming . . . video data" is "**video data prior to or during compression or decompression**

by the video codec." Further, the proper construction of the phrase "interim storage of incoming and outgoing video data" is "**temporary storage of video data prior to or during compression or decompression by the video codec and outgoing video data (as construed herein)**."

F. "Video Compressor/Decompressor Disposed Fully Within The Chip"

The precise term "video compressor/decompressor" appears only in the claims of the '788 Patent (*see, e.g.*, element [c] of representative claim 13). While not in the specification, there is much in the specification which sheds light on the meaning of this claim element. The specification states:

> Briefly, a video codec embodiment of the present invention comprises **video compression and decompression processors**, and **single-chip architectures** for intra-frame coding/decoding, discrete cosine transform, inter-frame coding and decoding, motion estimation, motion-compensated prediction, quantization, variable length coding and decoding and error detection and correction, and frame synchronization. Full-duplex video data bitstreams are simultaneously encoded and decoded with **shared resources**.

(Cockings Decl. Exh. A, 2:31-39.) The specification goes on to state:

> The video input/output buffer (VP) 30 is such that the incoming pixels are buffered and stored in the external DRAM 18 for raster-scan-to-block conversion. **Macroblocks of such pixel data are fetched and used for discrete cosine transform in intra-frame compression and for motion-estimation in inter-frame compression in the motion prediction processor (MP) 32.**
>
> **The discrete cosine transform and quantization (DCTQ) block 34 provides for discrete cosine transform, zigzag conversion and quantization, both forward and inverse.** For discrete cosine transforms, dedicated logic is used to do row and column transformations. Bits in the intermediate result are preserved for output coefficient precision that exceeds the ITU and IEEE standard requirements. Quantization logic makes the trade-off between spatial and temporal resolutions. Saturation logic is included to prevent overflow.

(*Id.* 4:63-5:10.) In further describing the operations associated with motion prediction processor 32, the specification states that when encoding it "computes the difference between two sequentially-adjacent video frames and supplies a frame-difference data, instead of the frame itself, to the DCTQ 34." (*Id.* 6:1-4.) Conversely, when encoding, it "reconstructs each video

frame by adding a received-frame difference to a frame prediction based on previous reconstructed frames." (*Id.* 6:10-12.) Figure 3 and its accompanying description teaches various details regarding the DCTQ block 34. (*See, e.g.*, *id*. 7:21-45.)

During the initial examination, in responding to an Official Action, the applicants stated:

> The essence of the claimed present invention is to provide for simultaneously encoding and decoding full-duplex video data bitstreams with **shared resources**. . . .
>
> . . . .
>
> The state of the art in the present subject matter is quite advanced, and the claimed present invention derives it principle novelty from using **shared resources** in the full-duplex communication of compressed and decompressed video information in a single chip.

(Cockings Decl. Exh. D, at 147-48 (Amendment Mar. 4, 1997).)

The specification and prosecution history show that the same circuitry (*i.e.*, "shared resources") is used for compression and decompression. And the plain language requires that this circuitry must be located entirely within the chip as recited.

Accordingly, in light of all of the foregoing, AVT respectfully submits that the term "video compressor/decompressor disposed fully within the chip" means "**circuitry located entirely within the chip (as construed herein) for video compression and decompression**."

G. "Dedicated Hardware Logic"

The phrase "dedicated hardware logic" appears twice in claim 13 as quoted above in element [e].

> **[e]** wherein the video compressor/decompressor includes **dedicated hardware logic** which performs forward discrete cosine transforms on the video information received from the video input connection and wherein the same **dedicated hardware logic** also performs inverse discrete cosine transforms on the video information received from the receive channel.

It is worthwhile to initially recognize that the "dedicated hardware logic" is something which is included as part of the "video compressor/decompressor." The "video

compressor/decompressor" is itself something that is recited by the claim to be disposed within the chip. In addition, "dedicated" does not require that the logic does only one thing, as in this element alone, the same hardware logic performs both discrete cosine transformation and inverse discrete cosine transformation.

Webster's defines the word "dedicated" as "devoted to a cause, ideal, or purpose." (Cockings Decl. Exh. G, at 589.) The technical *McGraw-Hill* dictionary defines "hardware" in the context of computer science as, "the physical, tangible, and permanent components of a computer or data processing system . . . ." (*Id.* Exh. H, at 904.) The *IEEE Dictionary* defines "hardware" as "physical equipment used to process, store, or transmit computer programs or data." (Cockings Decl. Exh F, at 584.) The final word in this term, "logic," has a variety of definitions, of which the most useful is that "logic" is a "general term for the various types of gates, flip-functions in a digital computer." (Cockings Decl. Exh. H, at 1164.)

As noted above, this dedicated hardware logic performs multiple functions. For example, as set forth in the representative claim 13, it "performs forward discrete cosine transforms on the video information received from the video input connection" and it also "performs inverse discrete cosine transforms on the video information received from the receive channel." Then, in claim 14 the same "dedicated" hardware performs "zigzag operations on the video information received from the video input connection and inverse zigzag operations on the video information received from the receive channel." And in claim 15, it additionally "performs quantization on the video information received from the video input connection and inverse quantization on the video information received from the receive channel."

The specification of the '788 Patent is fully consistent with this concept. Although the specification does not use the complete phrase "dedicated hardware logic," it does include a number of areas in which that concept is suggested. For example:

> The discrete cosine transform and quantization (DCTQ) block 34 provides for discrete cosine transform, zigzag conversion and quantization, both forward and inverse. For discrete cosine transforms, **dedicated logic is used to do row and column transformations**. Bits in the intermediate result are preserved for output coefficient precision that exceeds the ITU and IEEE standard requirements. Quantization logic makes the trade-off between spatial and temporal resolutions. Saturation logic is included to prevent overflow.

(Cockings Decl. Exh. A, 5:3-11.) Similarly, the specification states at a later point:

> As shown in FIG. 3, the DCTQ 34 includes **a first dimension (row) processor 80**, a row/column RAM (RCRAM) 81, and **a second dimensional (column) processor 82**. A DCTQ parameter register 83 is connected to the parameter address and data buses 50 and 52. A state machine 84 drives the processors 80 and 82. A zigzag (ZZ) unit 84 and a quantizer (Q) 86 complete the DCTQ 34. The DCTQ 34 is host-programmable by virtue of the parameter register 83, which allows for adaptive quantization and rate buffer control. This provides for the optimization of a variety of applications in different environments. In essence, problematic portions of each frame susceptible to compression artifacts are favored with a disproportionate share of the compressed bitstreams, thereby reducing compression-artifact generation. **DCTQ 34 includes high-speed algorithm specific processors that compute both the two-dimensional forward and inverse discrete cosine transform over eight-by-eight data blocks**.

(*Id.* 7:29-45.) Still further, at a later point in the specification, the following discussion appears:

> Each processor 80 and 82 includes arithmetic elements connected to the row-column memory 81. Each such arithmetic element includes a multiplier and two adders for computing an eight-point one-dimensional discrete cosine transform in sixteen clock cycles.

(*Id.* 7:56 to 8:4.)

Thus, given all of the foregoing, AVT respectfully submits that the appropriate construction of "dedicated hardware logic" is "**<u>specific integrated circuitry or circuit elements for the purpose of performing video compression and decompression</u>**."

H. "Communication Channel Bit Rates"

This term appears in the claims in context of "said transmit and receive channels have **communication channel bit rates** reduced by quantization and variable length coding." The plain language of this term indicates that the bit rates are associated with a communication channel. The surrounding claim language further links the term to the bit rates of the transmit and receive channels. Element [a] of claim 13 states that these channels are used to transmit and receive "compressed data." Further, element [c] informs us that this compressed data is output from the chip on the transmit channel and, conversely, compressed data is input into the chip on the receive channel.

The '788 Patent teaches that video information compressed by the video codec "is transmitted out in compressed form on a transmit channel." (Cockings Decl. Exh. A, Abstract.) Similarly, it also discloses that "compressed video information is input to the video codec from a receive channel." (*Id.*) The detailed description includes similar disclosure. (*Id.* 3:45-50.)

The plain meaning of claim language and specification therefore support AVT's construction that "communication channel bit rates" means "**the rate at which data bits are transmitted or received over the communication channel**."

I. "Quantization"/"Inverse Quantization"

The term "quantization" is used in element [d] of claim 13 (and each of the asserted claims):

> **[d]** wherein, said compression of video information is by spatial de-correlation of intraframe information and temporal decorrelation of interframe information, and said transmit and receive channels have communication channel bit rates reduced by **quantization** and variable length coding; and

Claim 15 also uses "quantization" in the context that the "dedicated hardware logic also performs **quantization** on the video information received from the video input connection." The context

of surrounding claim language of claims 13 and 15 further tells us that quantization is used in reducing the bit rates of the information received on the video input connection for output on the transmit channel.

Claim 15 also uses "inverse quantization" in the context of the dedicated hardware logic performing "**inverse quantization** on the video information received from the receive channel." A well understood meaning of the word inverse according to *Webster's* is "opposite." (Cockings Decl. Exh. G, at 1189.) The term "inverse" as a modifier to "quantization" indicates that whereas "quantization" reduces or compresses the bit rate, "inverse quantization" expands or decompresses it. In this regard, the language of claim 15 is instructive in that "inverse quantization" is used on video information being processed in the opposite direction, *i.e.*, compressed data on the receive channel being decompressed for output on the output connection.

The technical *McGraw-Hill* dictionary defines quantization in the context of data communications as "Division of the range of values of a wave into a finite number of subranges, each of which is represented by an assigned or quantized value within the subrange." (Cockings Decl. Exh. H, at 1620.) The *IEEE Dictionary* includes an almost identical definition: "**(3) (data transmission)**. In communications quantization is a process in which the range of values of a wave is divided into a finite number of smaller subranges, each of which represented by an assigned (or quantized value) within the subrange." (Cockings Decl. Exh. F, at 1046.)

These definitions are consistent with the use of the term in the specification. The specification further states that after thresholding, "the quantized coefficients are either *clipped* for an eight-bit range, or the de-quantized coefficient are *clipped* to a twelve-bit coefficient, depending on whether encoding or decoding." (Cockings Decl. Exh. A, 8:12-16.) The reference to "eight-bit range" during encoding refers to resolution of the values that the coefficients are

being converted to. This includes values within a range represented by eight-bit discrete values. By "clipping" the coefficients for these ranges, the quantization process converts the values to a finite number or discrete set of values that represent a reduction in the number of data bits. Decoding carries out the opposite process.

In view of the foregoing, AVT respectfully submits that the proper construction of the term "quantization" is "**conversion of data from a relatively large set to a smaller and discrete set**." In contrast, "inverse quantization" is construed to mean the opposite: "**conversion of data from a relatively small and discrete set to a larger set**."

J. "Receive Buffer"/"Transmit Buffer"

The terms "receive buffer" and "transmit buffer" appear in claim 23 in relation to how the dynamic random access memory (DRAM) is segmented. Specifically, the claim recites that the DRAM includes "segments for storage of video data compression and decompression frames, a **transmit buffer** and a **receive buffer**." The plain meaning of the claim language tells us that the DRAM is apportioned into different sections that include transmit and receive buffers.

The specification likewise states that "DRAM 18 is partitioned by the video codec into four sections: (1) an encoder frame buffer (EFB), (2) a decoder frame buffer (DFB), (3) a transmission channel buffer (TCB), and (4) a reception channel buffer (RCB)." (Exh. A 8:45-49.) The specification also refers to these buffers as the "encoding and decoding frame buffers, as well as the transmit and receive buffers." (*Id.* 5:32-33.) These references indicate that the transmit and receive buffers in the DRAM are associated with the transmit and receive channels. As explained above, these channels are configured to transmit and receive compressed video data. Therefore, the transmit/receive buffer are used to temporarily store compressed data transmitted or received on the respective channels.

Accordingly, AVT respectfully submits that the proper construction of "receive buffer" is "**portion of memory used to temporarily store received compressed video data** and "transmit buffer" is "**portion of memory used to temporarily store compressed video data to be transmitted**."

K. "Motion-Compensated Using Newly Computed Motion Vectors"

The term "motion-compensated using newly computed motion vectors" appears only in claim 5 as part of a wherein clause:

> wherein, motion estimation is provided for luminance data only, and motion vectors for chrominance data is about one-half of that for luminance data, for a particular macroblock of four luminance blocks and two chrominance blocks, such that a frame at "t-1" is **motion-compensated using newly-computed motion vectors** for both luminance and chrominance, and a motion-compensated frame "t-1" passed through an optional loop filter, is compared with a current frame "t";

The claim language "motion-compensated" in and of itself suggests compensating for motion. The surrounding claim language tells us "that *a frame at 't-1' is motion-compensated* using newly-computed motion vectors . . . and a *motion-compensated frame 't-1'* passed through optional loop filter." Earlier portions of the claim clarify that a frame at time "t-1" is the video frame earlier in time (or previous) to a current frame being processed. Therefore, the plain and ordinary meaning of the disputed claim language suggests that motion associated with a video frame is accounted for using motion vectors.

Other portions of the claim indicate that the motion-compensated frame occurs during "motion estimation." The specification teaches that motion estimation is part of the interframe compression process:

> In order to have a higher compression ratio, interframe compression is done taking advantage of the fact that adjacent frames are highly correlated temporally. Motion estimation uses two sequential frames, and motion vectors are then included in the encoded bit stream.

(Cockings Decl. Exh. A, 4:8-14.)

This portion of the specification further explains that interframe processing involves comparing the macroblocks of pixel data in the current and previous frames to determine how much the macroblocks change location or move between frames over time. (*Id.* 4:15-20, *see also* 6:62-65.) The specification also clarifies that the "array of processors 70 is used to concurrently find any motion vectors between current macro-blocks and previous macroblocks." (Cockings Decl. Exh. A, 14:24-28.) The amount of movement of the blocks of pixel data between frames is therefore tracked using motion vectors, which as explained in the Introduction above describes the direction and amount of movement of a picture between video frames.

Further, as explained in the background of the '788 Patent, "[m]otion prediction techniques encode motion vectors and compare the last frame sent, motion-compensated, to the current frame and take the difference." (*Id.* 33-35.) Thus, a "motion-compensated" frame of video is represented by a motion vector that tells how much a particular macroblock of pixels moves between frames. Therefore, the entire phrase should be interpreted to reflect the plain meaning and the description provided within the specification.

In view of all of the foregoing, AVT respectfully submits that in light of the claim language, the plain and ordinary meaning of the term "motion-compensated using newly-computed motion vectors" is "**compensating for the movement of pixel blocks between video frames using motion vectors computed based on the movement between frames**."

L. "As Simple As An Absolute Difference"

With respect to the asserted claims, the term "as simple as an absolute difference" appears in claim 5 in reference to determining a motion vector:

> wherein the video compressor/decompressor includes a process for comparing the macro blocks for the current frame at a time "t" with the macro blocks of a previous frame "t-1", and a displacement vector within a defined search window that provides a minimum cost function, which can be **as simple as an absolute difference**, is the motion vector and is encoded by variable length coding;

The context of the surrounding claim language informs us that the "absolute difference" is used in calculating displacement of blocks of video data in the current frame relative to a previous frame in time. Further, this displacement is captured in a vector that "provides a minimum cost function" within a search window.

As explained in the '788 Patent specification, a "search window 76 contains several macroblocks." (Cockings Decl. Exh. A, 5:61-63.) It also explains that the cost function is calculated as part of motion estimation. (*Id.*, 5:63-66.)

As part of motion estimation the macroblocks within a "window" are searched to find a best matching macroblock. As explained in preceeding Subpart III.K, in processing a sequence of video frames macroblocks of pixel data in the current frame in time are compared to macroblocks in a previous frame. (*Id.* 4:15-17; 6:1-9) As part of this processing, "the motion predictor 32 computes the difference between two sequentially-adjacent video frames and supplies a frame difference data." (*Id.* 6:1-4.) The difference data reflects how much a macroblock in the current video changes relative to the same macroblock in the previous frame.

The specification closely tracks the claim language in explaining that the "displacement vector within a defined search window (a maximum of 46^2 in H. 261) that provides a minimum cost function which can be as simple as an absolute difference is the motion vector." (*Id.* 4:17-20.) The minimum cost function refers to the number of computations required to search a target macroblock within a search window. (*Id.* 6:28-31.) Examples of such computations including subtractions, determining the magnitude or absolute differences associated with a macroblock, and accumulating or summing the differences between the pixel locations. (*Id.*)

Accordingly, to one of ordinary skill in the art, the specification teaches that the term "as simple as an absolute difference" means "**the sum of the magnitude of differences between pixel locations**."

V. CONCLUSION

AVT respectfully submits that the claim constructions it has urged above are faithful to the intrinsic evidence; namely, the claims themselves, the specification, and the prosecution history of both the original application and the reexamination. They also make appropriate use of the most reliable and credible form of extrinsic evidence; namely, general purpose and technical dictionaries.

Respectfully submitted,

LERNER, DAVID, LITTENBERG,
KRUMHOLZ & MENTLIK, LLP
Attorneys for Plaintiff Advanced Video Technologies LLC

Dated: May 11, 2012

By: s/ Orville R. Cockings
Orville R. Cockings
Tel: 908.654.5000
E-mail: ocockings@ldlkm.com
litigation@ldlkm.com